

**Digital Design II**

**Project 1**

**Final Report**

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**Overview**

In this project, we designed (schematic and layout), verified, and characterized a standard cell library composed of 16 different cells, representing 5 different functions as follows:

1) Inverter (sizes: 1, 2, 4 and 8)

2) Tri-state Inverter (sizes: 1, 2, 4 and 8)

3) 2 input NAND gate (sizes: 1, 2 and 4)

4) 2 input NOR gate (sizes: 1, 2 and 4)

5) The complex function: (𝑥, 𝑦, 𝑧,𝑤) = ~(𝑥𝑦+𝑤𝑧), (sizes: 1 and 2)

Our standard cell library has the following properties:

* It uses lambda-based design rules.
* Cell height = 120 λ
* N-well height = 70 λ
* Site width = 4 λ

Stick diagrams were designed for each function, as well as transistor-level circuits and layout.

Each cell was verified by trying all different combinations of input voltages.

Also, for each cell, a total of 16 simulations were run, recording values of propagation delays (both rising and falling) for different values of loading and input transition. In addition, a linear delay model for each of rising delay and falling delay was derived. These results are shown in the upcoming characterization section.

**Procedure**

For each cell, a set of defined steps were taken:

1. A transistor schematic was designed on Electric VLSI, sized according to the models taken in lecture. This schematic was verified using spice comprehensive simulation. A basic template for verifying cells was developed to this end (spice\_snippet\_v.txt).
2. The transistor sizing was fine-tuned to be as symmetric as possible. To do this, a process of trial and error was undertaken. A basic spice template was developed to ease the measurements process (measuring all needed values for each cell in one spice deck) (spice\_snippet.txt). This template also measures the differences between rising and falling delays for the same loading and input transition conditions. A python script was developed to compute the average of these differences, their standard deviations, and the linear delay models for the cells (linear\_model.py). The best sizing conditions were chosen to the end of minimizing the (absolute) value of the differences average and their standard deviation.
3. The stick diagram was developed.
4. The layout was developed on Electric VLSI. Each cell was designed with an aim to minimize height. The tallest cell, which defined the height for the library, was the size 8 tri-state inverter (120 λ). The n-well height was also determined from the same cell (70 λ).